

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

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1           1. (Currently Amended) A digital system comprising a  
2 microprocessor having an instruction execution pipeline with a  
3 plurality of pipeline phases, wherein the microprocessor comprises:  
4           program fetch circuitry operable to perform a first portion of  
5 the plurality of pipeline phases;  
6           instruction decode circuitry connected to receive fetched  
7 instructions from the program fetch circuitry, the instruction  
8 decode circuitry operable to perform a second portion of the  
9 plurality of pipeline phases; and  
10          at least a first functional unit connected to receive a  
11 plurality of control signals from the instruction decode circuitry,  
12 the functional unit operable to perform a third portion of the  
13 plurality of pipeline phases, the third portion being execution  
14 phases, wherein the first functional unit comprises:  
15          first test circuitry connected to receive an operand from a  
16 selected test register, and having an output for indicating a  
17 condition of the operand;  
18          decrement circuitry connected to receive the operand from the  
19 selected test register, and having an output connected to  
20 conditionally provide a decremented value of the operand to the  
21 test register dependent upon said indicated condition of the  
22 operand;  
23          adder circuitry connected to receive a program counter value  
24 and a displacement value, and having an output connected to  
25 conditionally provide a branch address to a program counter  
26 register dependent upon said indicated condition of the operand;  
27 and

28 wherein the first test circuitry, the decrement circuitry, and  
29 the adder circuitry are all operable to test the operand,  
30 conditionally decrement the operand, and conditionally provide a  
31 branch address to the program counter in response to a single  
32 conditional branch-decrement instruction ~~of a first type~~.

1 2. (Currently Amended) The digital system of Claim 1,  
2 wherein the first test circuitry, the decrement circuitry, and the  
3 adder circuitry are all operable to test the operand, conditionally  
4 decrement the operand, and conditionally provide a branch address  
5 to the program counter in response to a single conditional branch-  
6 decrement instruction during a single one of the third portion of  
7 pipeline phases.

3. (Canceled)

1 4. (Original) The digital system of Claim 3, further  
2 comprising second test circuitry connected to test a condition of a  
3 selected predicate register, and having an output for indicating a  
4 condition of the predicate register, wherein the second test  
5 circuitry is operable to inhibit the program counter from receiving  
6 the branch address if the contents of the predicate register do not  
7 correspond to a second condition.

Claims 5 to 9. (Canceled)

1 10. (Currently Amended) A method of operating a digital  
2 system having a microprocessor with a conditional ~~branch~~ branch-  
3 decrement instruction, comprising the steps of:  
4 fetching a conditional ~~branch~~ branch-decrement instruction for  
5 execution;

6 testing a test register selected by the conditional ~~branch~~  
 7 branch-decrement instruction to determine if the contents of the  
 8 test register meet a first condition;  
 9 providing a branch address to a program counter to cause a  
 10 branch if the contents of the test register meet the first  
 11 condition; and  
 12 <sup>cond</sup> modifying the contents of the test register <sup>only</sup> if the contents of  
 13 the test register meet the first condition. <sup>this indicates the modification since it is performed after the branch step</sup>

1. met by subsequent modification of test register.

1 11. (Amended) The method of Claim 10, further comprising the  
 2 steps of:

3 testing a predicate register selected by the conditional  
 4 ~~branch~~ branch-decrement instruction to determine if the contents of  
 5 the predicate register meet a second condition; and  
 6 inhibiting the step of providing a branch address to the  
 7 program counter and inhibiting said step of modifying the contents  
 8 of the test register if the contents of the predicate register do  
 9 not meet the second condition.

1 12. (Original) The method of Claim 10, wherein the step of  
 2 modifying decrements the test register.

1 13. (Original) The method of Claim 10, wherein the steps of  
 2 testing, providing, and modifying are all performed during a same  
 3 execution phase of the microprocessor.

14. (Canceled)

1 15. (New) The digital system of Claim 1, further comprising:  
 2 a register file including a plurality of general purpose  
 3 registers, each general purpose register capable of supplying an

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4 operand to a functional unit and capable of receiving destination  
5 data generated by a functional unit; and  
6 wherein said conditional branch-decrement instruction  
7 designates one of said general purpose registers as said selected  
8 test register.

1 16. (New) The digital system of Claim 15, further comprising:  
2 second test circuitry connected to test a condition of a  
3 selected predicate register, and having an output for indicating a  
4 condition of the predicate register, wherein the second test  
5 circuitry is operable to inhibit the program counter from receiving  
6 the branch address and inhibit said step of modifying the contents  
7 of the test register if the contents of the predicate register do  
8 not correspond to a second condition; and  
9 wherein said conditional branch-decrement instruction  
10 designates one of said general purpose registers as said predicate  
11 register.

1 17. (New) The digital system of Claim 16, wherein:  
2 said conditional branch-decrement instruction designates one  
3 of said general purpose registers of a predetermined subset of said  
4 general purpose registers as said predicate register.

1 18. (New) The digital system of Claim 1, wherein:  
2 said program fetch circuitry operable to fetch a fetch packet  
3 of a predetermined plurality of instructions each first portion of  
4 the plurality of pipeline phases starting at predetermined address  
5 boundaries; and  
6 said adder circuitry adds said displacement value to said  
7 predetermined address boundary of said fetch packet containing said  
8 conditional branch-decrement instruction.

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1 19. (New) The digital system of claim 18, wherein:  
2 said instruction decode circuitry reads a predetermined bit of  
3 each instruction to determine an execute packet of instructions  
4 capable of execution in parallel on a plurality of functional  
5 units, wherein an execute packet may include instructions in two  
6 sequential fetch packets; and  
7 said adder circuitry adds said displacement value to said last  
8 predetermined address boundary of a second sequential fetch packet  
9 if said second sequential fetch packet contains said conditional  
10 branch-decrement instruction.

1 20. (New) The method of Claim 10, further comprising the step  
2 of:  
3 storing data in a register file including a plurality of  
4 general purpose registers;  
5 recalling data from an instruction designated general purpose  
6 register for supplying an operand to a functional unit;  
7 storing destination data generated by a functional unit in an  
8 instruction designated general purpose register; and  
9 designating via the conditional branch-decrement instruction  
10 one of said general purpose registers as said selected test  
11 register.

1 21. (New) The method of Claim 20, further comprising:  
2 testing a predicate register selected by the conditional  
3 branch-decrement instruction to determine if the contents of the  
4 predicate register meet a second condition; and  
5 designating via the conditional branch-decrement instruction  
6 one of said general purpose registers as said predicate register.

AW 1 22. (New) The method of Claim 21, wherein:  
2 said step of designating said predicate register designates  
3 said predicate register from a predetermined subset of said general  
4 purpose registers as said predicate register.

1 23. (New) The method of Claim 10, wherein:  
2 said step of fetching instructions fetches a fetch packet of a  
3 predetermined plurality of instructions; and  
4 said step of providing a branch address to the program counter  
5 adds a displacement value to said predetermined address boundary of  
6 said fetch packet containing said conditional branch-decrement  
7 instruction.

1 24. (New) The method of claim 23, wherein:  
2 reading a predetermined bit of each instruction to determine  
3 an execute packet of instructions capable of execution in parallel  
4 on a plurality of functional units, wherein an execute packet may  
5 include instructions in two sequential fetch packets;  
6 dispatching each instruction of each execute packet to a  
7 corresponding functional unit in parallel;  
8 said step of providing a branch address to the program counter  
9 adds said displacement value to said last predetermined address  
10 boundary of a second sequential fetch packet if said second  
11 sequential fetch packet contains said conditional branch-decrement  
12 instruction.